Express Mail Label No. EV 225206709 US
Date of Deposit: April 15, 2004
Atty. Docket No. 112020.128 US2 (NAN-5CON)

Methods of Making Electromechanical Three-Trace Junction Devices

Cross Reference to Related Applications

[0001] This application is a continuation of and claims priority to U.S. Patent Application No. 10/033,032 filed on December 28, 2001, now Patent No. 6,784,028 entitled METHODS OF MAKING ELECTROMECHANICAL THREE-TRACE JUNCTION DEVICES, which is related and claims priority to the following applications, the contents of which are incorporated herein in their entirety by reference:

U.S. Patent Application No. 09/915,093 filed July 25, 2001, entitled ELECTROMECHANICAL MEMORY ARRAY USING NANOTUBE RIBBONS AND METHOD FOR MAKING SAME;

U.S. Patent Application No. 09/915,173 filed July 25, 2001, entitled ELECTROMECHANICAL MEMORY HAVING CELL SELECTION CIRCUITRY CONSTRUCTED WITH NANOTUBE TECHNOLOGY;

U.S. Patent Application No. 09/915,095 filed July 25, 2001, entitled HYBRID CIRCUIT HAVING NANOTUBE ELECTROMECHANICAL MEMORY.

Background

1. Technical Field

[0002] This invention relates in general to nonvolatile memory devices and, in particular, to nonvolatile memory arrays that use electromechanical nanotube technology.

2. Discussion of Related Art

[0003] Typical memory devices involve single-bit memory cells that have either an "on" state or an "off" state. One bit of memory storage is determined by either the "on" or "off" condition. The number of bits is dependent directly upon the number of memory cells in a particular memory array. For example, a device, which stores *n* bits, must have *n* memory cells. In order to increase the number of memory cells either the overall size of the memory array must increase or the size of each memory element must decrease. Increases in memory cell density have been achieved by improving lithographic